IN THE CLAIMS

1. (Previously Presented) A fuse element formed on a semiconductor substrate, the substrate having a standard subset of integrated circuit elements thereon all having a minimum design width produced by photolithography and that receive first and second power supply voltages, a conductive line formed on said substrate and having two end portions for connecting two adjacent photolithography produced features on said semiconductor substrate receiving respective said first and second power supply voltages, said conductive line further having a center portion with said two end portions and said center portion having said minimum design width, said conductive line further having a link portion formed approximately at the center of said center portion and spaced from said end portions which has a sub-minimum width less than said minimum design width, wherein said center portion is spaced from said two end portions by a spacing equal to at least twice said minimum design width, and the two minimum design width end portions and the sub-minimum width link portion are produced simultaneously in one photolithographic operation, and an application of said first and second power supply voltages across said end portions causes an electrical property of said fuse element to undergo a detectable change, wherein said spacing between said center portion and the end portions is sufficient to prevent the end portions from serving as a heat sink to increase the amount of joule heating required to change the electrical property.

2. (Original) The fuse element and semiconductor substrate of claim 1, wherein the conductive line includes a silicide thereon.

3. (Original) The fuse element and semiconductor substrate of claim 2, wherein the changed electrical property is resistance of the conductive line.

4. (Withdrawn) The fuse element and semiconductor substrate of claim 1, wherein the conductive line comprises a silicided gate of an FET, having an underlying doped poly.

5. (Withdrawn) The fuse element and semiconductor substrate of claim 4, wherein the changed electrical property is resistance of the FET.

6. (Withdrawn) The fuse element and semiconductor substrate of claim 4, wherein the changed electrical property is a threshold voltage of the FET.

7. (Canceled).

8. (Canceled).

9. (Canceled).

10. (Original) The fuse element and semiconductor substrate of claim 1, including a polysilicon E-Fuse which includes a narrow sub-minimum width polysilicon line to provide increased self heating during programming when a current is passed through the E-Fuse.

11. (Original) The fuse element and semiconductor substrate of claim 10, wherein the polysilicon E-fuse uses a shorted/open line to distinguish a programmed/unprogrammed E-Fuse.

12. (Original) The fuse element and semiconductor substrate of claim 10, wherein the polysilicon E-fuse uses a change in resistance to distinguish a programmed/unprogrammed E-Fuse.

13. (Withdrawn) The fuse element and semiconductor substrate of claim 1, including a work function altered MOSFET self–aligned E-Fuse which includes a narrow sub-minimum width polysilicon line to provide increased self heating during programming when a current is passed through the E-Fuse, which drives dopant from the narrow polysilicon line, self-aligning an active area to this region, which causes a significant decrease in current through the MOSFET E-Fuse, to distinguish an unprogrammed/programmed E-Fuse.

14. (Withdrawn) The fuse element and semiconductor substrate of claim 1, including a MOSFET wherein increasing the field in a local region of a channel of the MOSFET causes a low voltage snapback in the MOSFET, which significantly increases the current flow through the MOSFET, such that the device is fused from drain to source, enabling the device to be used as an anti-E-Fuse.

15. (Withdrawn) The fuse element and semiconductor substrate of claim 1, including a MOSFET wherein increasing the field in a local region of a channel of the MOSFET causes allow voltage snapback in the MOSFET, and which includes a narrow sub-minimum width

polysilicon line which allows for self-aligning source and drain contacts in a snapback region which provide a design for handling high program currents.

16. (Withdrawn) A mask used to form a sub-minimum image, comprising a first minimum size feature, and a second minimum size feature that is offset and spaced from said first minimum size feature.

17. (Withdrawn) A process of forming a sub-minimum size feature on a substrate, comprising:

forming a photosensitive polymer on the substrate;

exposing said photosensitive polymer to actinic radiation through a mask having a first minimum size feature and a second minimum size feature that is offset and spaced from said first minimum size feature; and

developing said polymer such that said sub-minimum size feature is defined by a portion of the mask between said minimum size features.

18. (Withdrawn) The process of claim 11, including forming an FET link as the sub-minimum feature.

19-20 (Canceled).